Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A0**
2. **B0**
3. **N.O0**
4. **A1**
5. **B1**
6. **N.O1**
7. **GND**
8. **N.O3**
9. **B3**
10. **A3**
11. **N.O2**
12. **B2**
13. **A2**
14. **VCC**

**DIE ID**

**AC00S**

**8 7 6**

**5**

**4**

**3**

**2**

**13 14 1**

**9**

**10**

**11**

**12**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0029” X .0029”**

**Backside Potential: GND (or leave FLOATING)**

**Mask Ref: AC00S**

**APPROVED BY: DK DIE SIZE .027” X .031” DATE: 12/4/17**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54AC00**

**DG 10.1.2**

#### Rev B, 7/19/02